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A Microelectronic Analog-to-Digital Converter and Sync Generator

J. Denton Allen

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

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J. Denton Allen

(NASA Contract NAS7-100)

Raymond L. Heacock, Chief
Space Instruments Development Section

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
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ABSTRACT

This Report describes the application of thin film passive components and planar transistor technology to the fabrication of an analog-to-digital converter and sync generator for use in spacecraft television. The analog-to-digital converter selected is described and compared with other types that were considered. Fabrication technology is discussed, and material selection criteria presented. It is concluded that the combination of semiconductor and thin film techniques discussed offers considerable advantages in this and other microelectronic applications.

I. INTRODUCTION

The work described in this Report was sponsored by the Jet Propulsion Laboratory (JPL) and carried out by Electro-Optical Systems (EOS) Inc., Pasadena, California. The ideas and techniques described resulted from an earlier microelectronics study program carried out by EOS for JPL (Ref. 1). As a result of these programs, the principal shortcomings of microelectronics techniques were determined.

Thin film microelectronic techniques are capable of providing passive components, having properties equal to or superior to those of conventional components. However, thin film amplifying devices have very poor performance characteristics. Semiconductor functional electronic blocks contain transistors and diodes which provide active elements having high performance characteristics, but their overall performance suffers when compared with similar circuits using conventional components because of the poor characteristics of the resistors and capacitors fabricated from semiconductor materials. Planar diffused diodes and transistors, therefore, were used for the active elements and on top of the oxide film, which is used to protect the active devices, thin film resistors and capacitors were deposited. Tantalum (Ta) was selected for the thin film components, since resistors and capacitors can be readily formed from it (Ref. 2).

To demonstrate the capabilities of this technique it was decided to apply it to some potentially flyable hardware, the design and fabrication of a 6-bit analog-to-digital converter (ADC). In designing this converter, special consideration was given to the fact that the circuits were to be fabricated in microelectronic form. The design of the converter is described and the fabrication techniques used to make the microcircuits are discussed in the remainder of this Report. The analog-to-digital converter forms the major part of a complete encoder designed to be compatible with the Mariner Mars 1964 television subsystem.

II. ANALOG-TO-DIGITAL CONVERTER

The analog-to-digital converter is required to carry out a 6-bit conversion for a system having a video frequency bandwidth of at least 7 kc. This requires one 6-bit conversion every 72 μsec. In addition, various synchronizing signals are required by the camera. Three methods of analog-to-digital conversion were originally considered for investigation in this program.

a. The ramp method.

b. The weighted adder successive approximation method.

c. The comparison amplifier method.

It was decided not to direct any effort to the ramp approach in this program, since it had already been fully investigated using TI 5100 series integrated circuits (Ref. 3). Accordingly, an analysis was made of the two latter methods to determine the accuracy requirements for the components in each of these systems. It was found that for a 6-bit conversion with the comparison amplifier approach the maximum gain error permissible per stage is 0.025%, and the maximum offset voltage error is 0.063 mv per stage. These requirements are too stringent for reasonable implementation. It is probable that a 4-bit system could be implemented, since the accuracy requirements would be 0.5% and 10 mv respectively.

The appendix discusses the weighted adder successive approximation approach. The analysis assumes that a 5 v input signal is to be digitized. A ½-bit error at the output of the weighted adder network is equivalent to a signal of 39 mv. If it is assumed that a power supply regulated to 0.1% is available, and that the transistor switches which feed the weighted adder have offset voltages of 8 mv or less, then the voltage errors arising will amount to 8.53 mv. The errors which arise due to variations of the resistors in the weighted adder network from their nominal value depend on the position of the resistor in the network. A 1% variation in resistance for the resistor in the most critical position gives rise to a voltage error of approximately 11 mv. Assuming these errors to be additive, the total error is 19.5 mv. If it is assumed that the signal source impedance, the weighted adder output impedance and the amplifier input impedance are equal and that the amplifier following the weighted adder chain can discriminate voltage differences of 7 mv, the maximum error will be less than ½ bit, which is allowed. This analysis shows that the accuracy requirements for the weighted adder successive approximation approach can reasonably be expected to be met by circuits fabricated by microelectronic techniques. It was decided, therefore, that this approach would be followed.

Figure 1 shows the overall sequencing logic for the analog-to-digital converter, and Fig. 2 shows the logic employed in the actual analog-to-digital conversion. In this scheme, the output of the digital-to-analog converter is compared to the analog input signal. The initial output of the analog-to-digital converter corresponds in magnitude to a voltage of ½-full scale. If the analog input exceeds ½-full scale voltage, the most significant digit is set up in a register. The voltage then corresponding to ¼-full scale is added to the ½-full scale voltage and a further comparison is made; however, if the analog voltage is less than ½-full scale, the most significant digit in the register is set to 0, the ½-full scale voltage is removed from the output of the digital-to-analog converter, and the ¼-full scale voltage then appears, whereupon a further comparison is made. This process is continued until all 6 digits have been set up. The output of the register is then read out by gating with appropriate digit pulses and appears in serial form.

The logic shown in Fig. 1 and 2 carries out one 6-bit conversion every 72 μsec. Note that this scheme is capable of carrying out one conversion every 12 μsec without requiring any increase in the speed of the circuitry, making it potentially suitable for systems requiring bandwidths in excess of 40 kc. The total power consumption of this system when fabricated in the breadboard stage is less than 1 w.

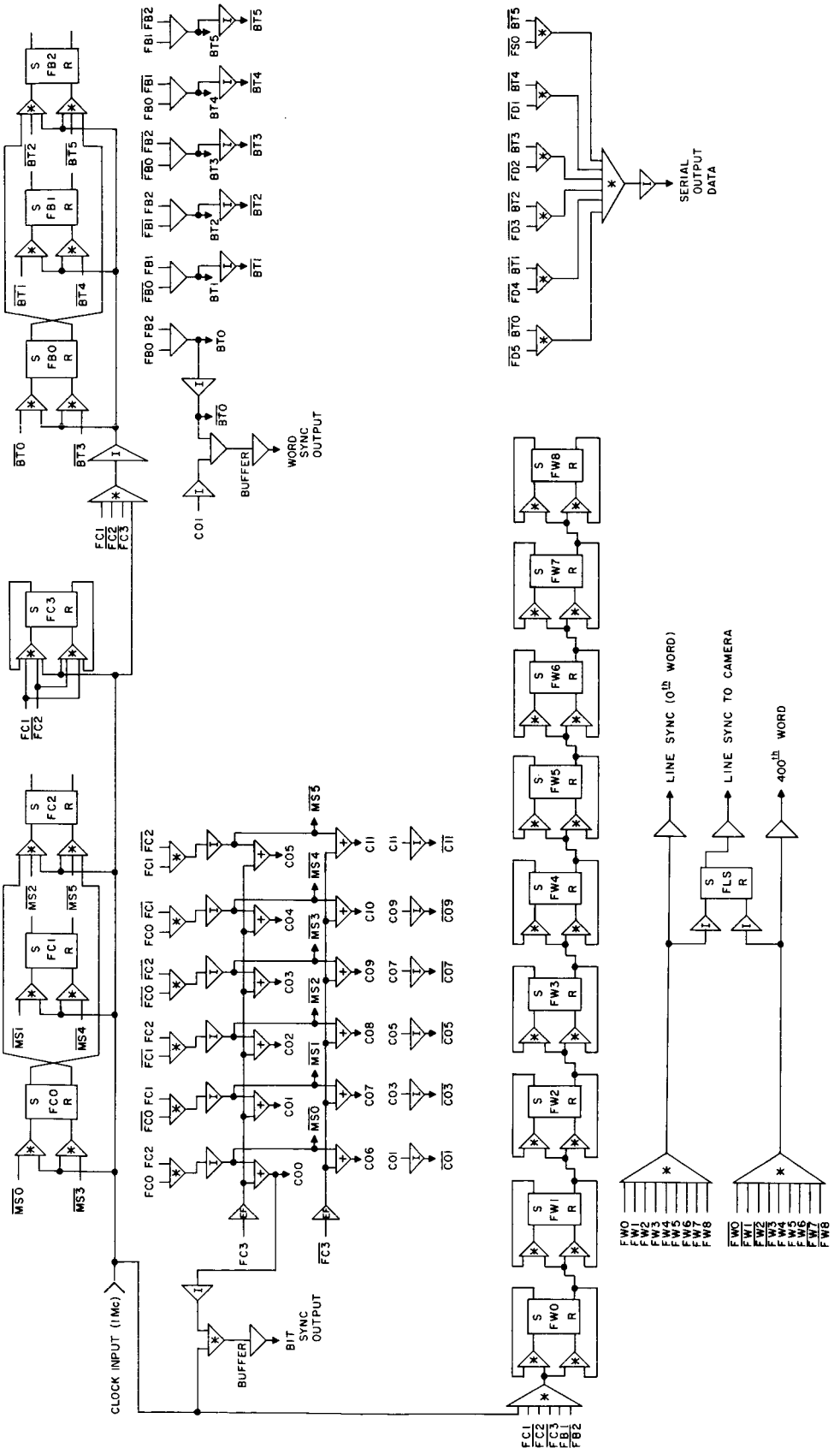


Fig. 1. Block diagram for overall sequencing logic

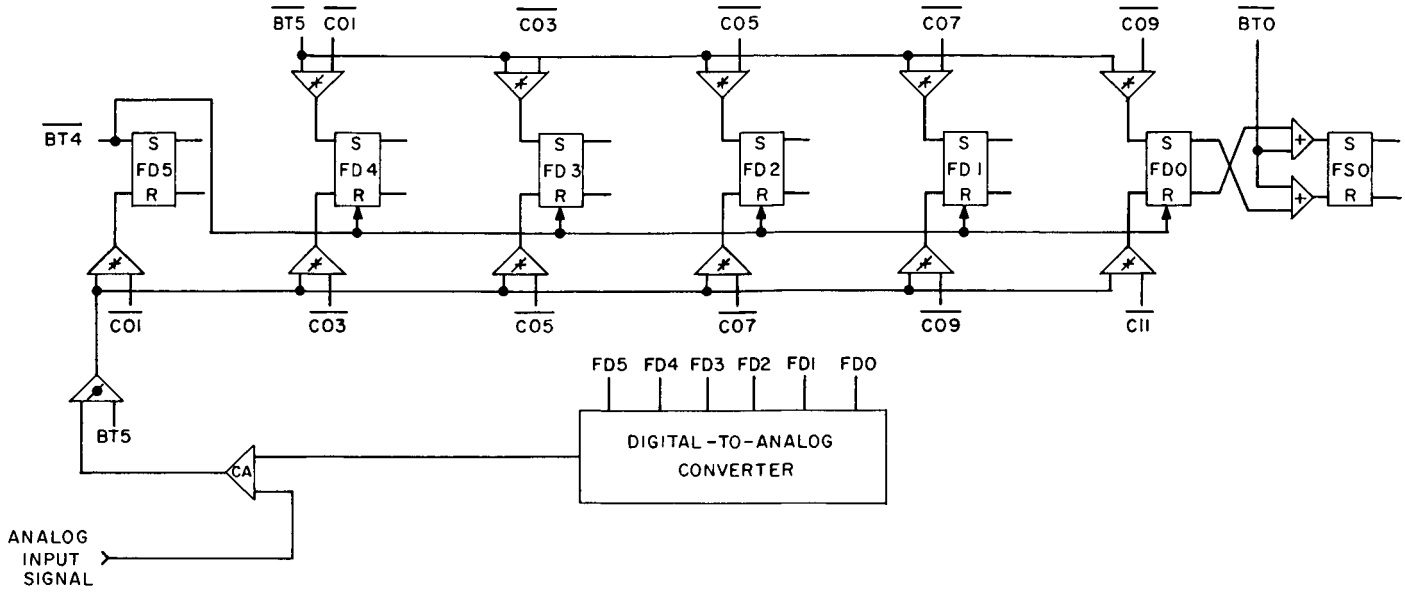


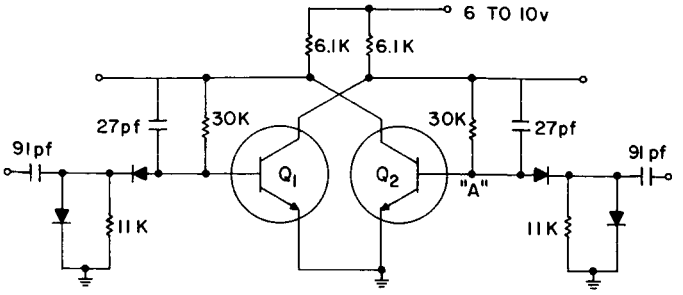
Fig. 2. Analog-to-digital converter, successive approximation approach

III. CIRCUIT DESIGN

The circuits required to implement the analog-to-digital conversion scheme discussed in section 2 are shown in Fig. 3–8. Each of these basic circuits meets two design considerations. First, the circuits are able to perform the electrical functions required of them. Second, the range of component values employed is such that the circuit can be fabricated using microelectronic techniques.

Figure 3 shows the set-reset type flip-flop which consumes 8 mw when operated with a supply voltage of 6 v. The gate circuits are shown in Fig. 4. These are arranged so that each circuit package contains either two 2-input gates or one 4-input gate. Notice also that there are additional input circuits, required when the gate is used as an inverter to drive the low level transistor switches, as in Fig. 5. Figure 6 shows a high power inverter and an emitter follower. Figure 5 is the low-level switch used for applying voltages to the weighted adder network, shown in Fig. 7. The last circuit, which occurs only once, is the comparison amplifier, shown in Fig. 8. All the circuits shown have been fabricated in breadboard form and a complete working analog-to-digital converter assembled. It is planned to replace these circuits with their microelectronic versions.

Since the flip-flops and gates occur most frequently, there being 24 flip-flops and 83 gates required in this system, it is planned to fabricate these two types of circuits first and insert them into the system. Since the gate will also act as a low power inverter, most of the 24 inverter circuits can also be implemented into microelectronic form. The conversion of the flip-flops and gates from conventional circuitry to microcircuitry will mean that approximately 90% of the analog-to-digital converter will be fabricated in microelectronic form.



TO POINT "A" CONNECT THE FOLLOWING CIRCUIT FOR A RESET LINE

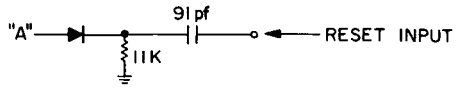
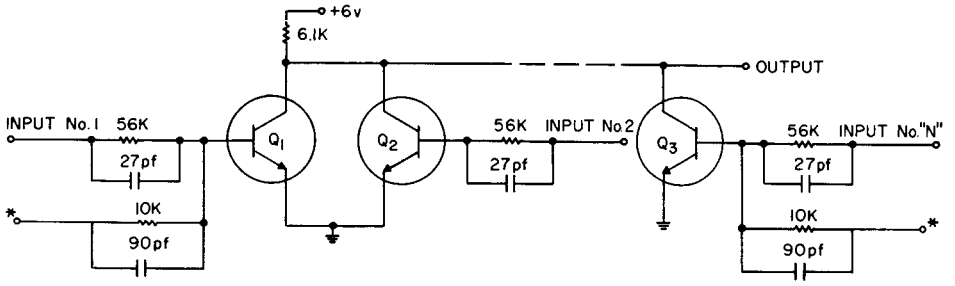


Fig. 3. Flip-flop low power 300 kc



*INPUT CIRCUIT WHEN GATE IS USED AS AN INVERTER

PRESENT REQUIREMENTS
2-9 INPUT *NOR* GATES
2-6 INPUT *NOR* GATES
3-4 INPUT *NOR* GATES
MORE THAN 10-3 INPUT *NOR* GATES
MORE THAN 10-2 INPUT *NOR* GATES

Fig. 4. *NOR* gates

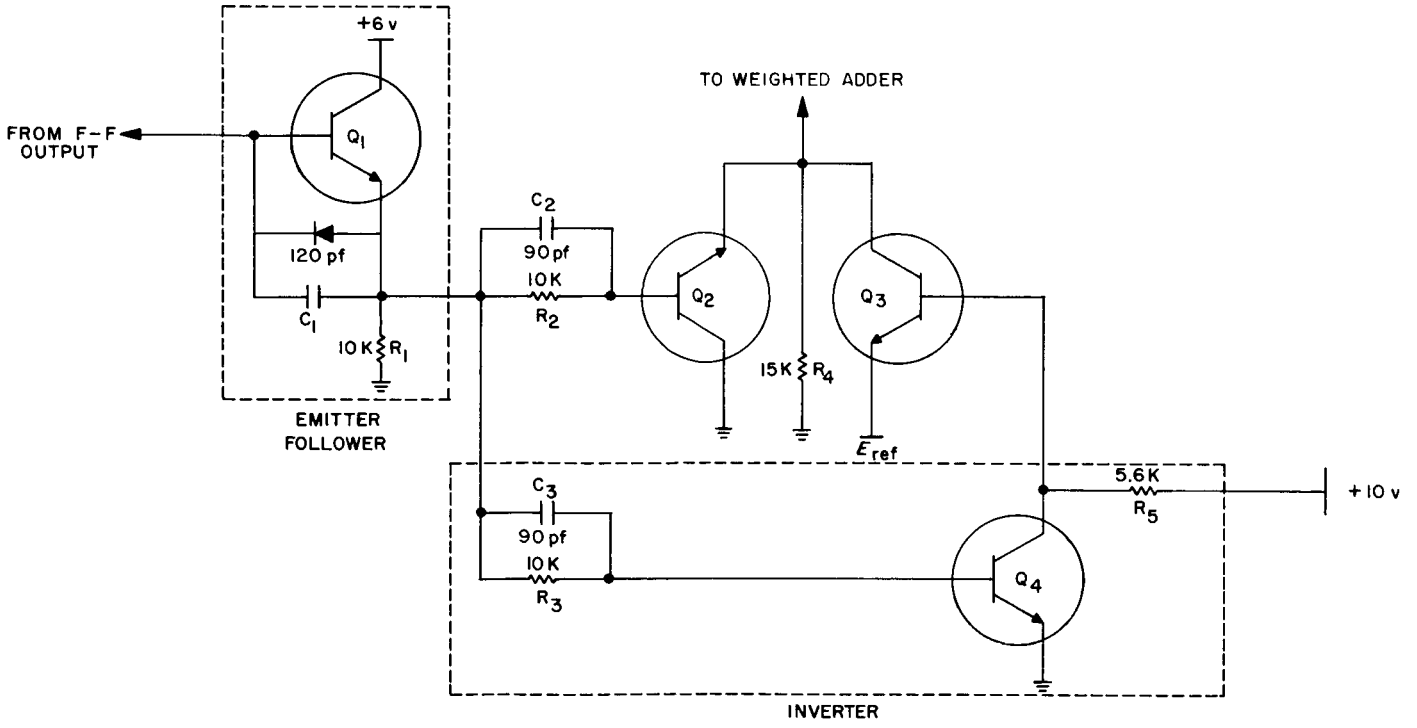


Fig. 5. Solid state switch

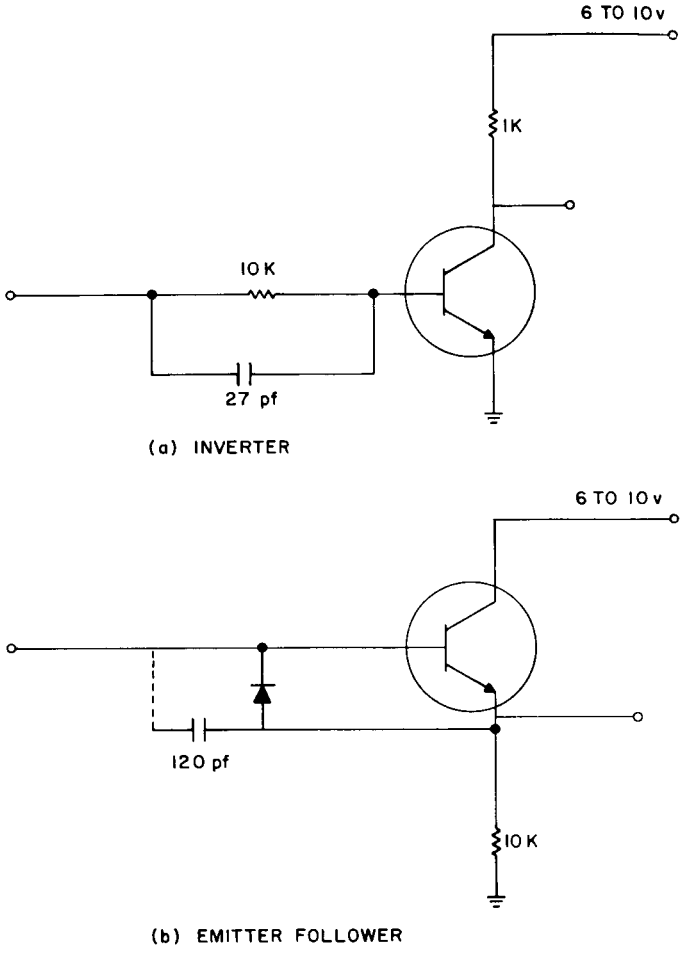


Fig. 6. High power inverter and emitter follower circuits

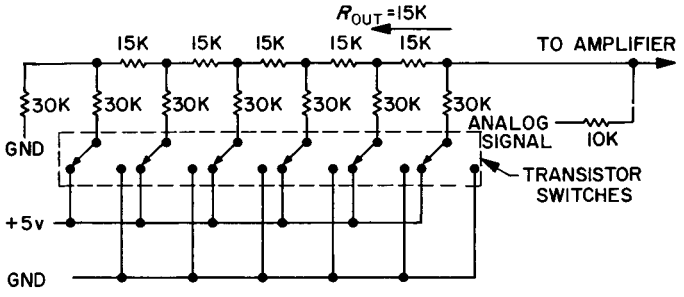


Fig. 7. Weighted adder network

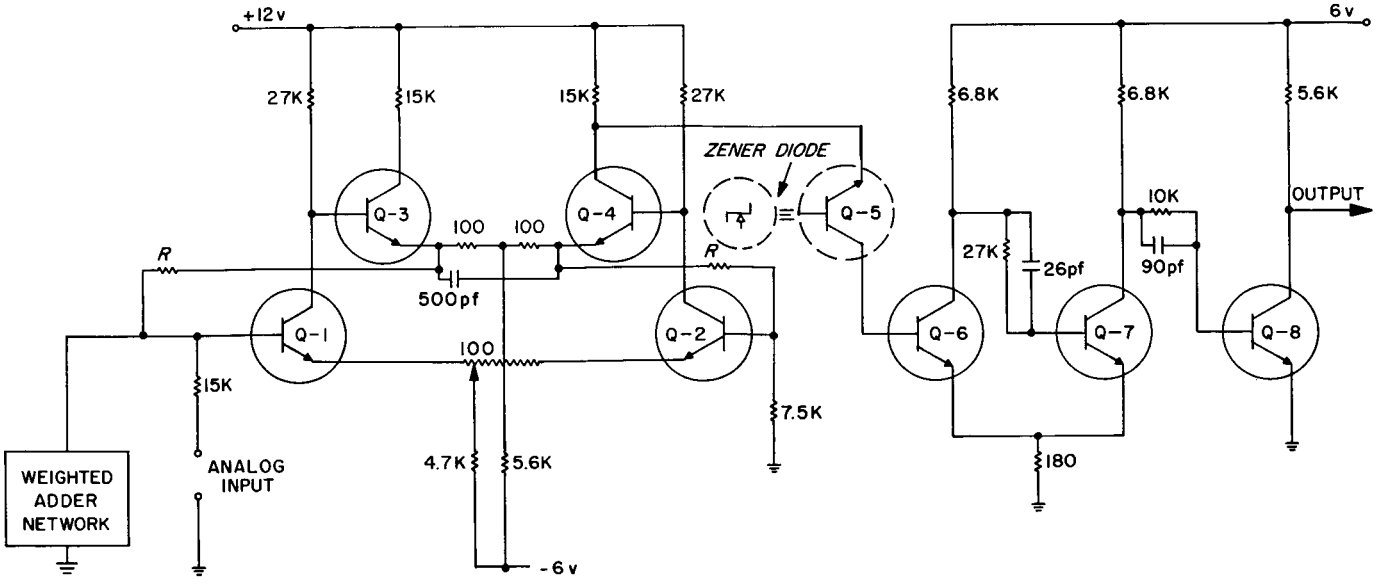


Fig. 8. Comparator amplifier (differential input)

IV. SELECTION OF MATERIALS FOR MICROCIRCUIT FABRICATION

The fabrication of microcircuits requires both active and passive devices. Past experience shows that resistors and capacitors having good electrical properties, long-term stability, and low temperature coefficients can be fabricated by thin film techniques. In order to provide amplification and rectification, it has been necessary, when using thin film components, to insert separately manufactured transistors and diodes by a welding or soldering process. This type of operation, which involves handling of individual components and manual joining, is undesirable from both cost and reliability points of view.

An alternative approach is to fabricate all components from a semiconductor, usually silicon. In this scheme, the transistors and diodes are fabricated using conventional diffusion techniques. Resistors are formed either by utilizing the bulk properties of the silicon or by diffusing areas of controlled configuration. This latter approach is usually adopted. Capacitors can be formed by using either reverse biased p-n junctions, or by using the dielectric properties of the thermally produced silicon oxide on the surface of the wafer. The transistors and diodes formed in this way are substantially equivalent in performance to their discrete counterparts, although some degradation may occur due to the addition of parasitic capacitances. The properties of the passive components compare unfavorably with both thin film and discrete components. It was decided, as a result of previous work, to utilize a combination of thin film and semiconductor techniques. The semiconductor chosen was silicon, since the techniques for fabrication of transistors and diodes by the use of oxide masked diffusion were already very highly developed (Ref. 4). In addition, since silicon is readily thermally oxidized to form an insulating layer of SiO_2 on the surface, it was felt that this oxide layer would provide a suitable substrate for the subsequent deposition of thin film passive components. Table 1 lists the properties of a number of metals that might be used for the fabrication of thin film resistors (Ref. 5). Table 2 shows the properties of a number of oxides that can be used for capacitor dielectrics. Table 3 shows the additional properties of some further materials for use as resistors and capacitors (Ref. 6). It is desirable that the material have a high resistivity and a low temperature coefficient of resistance. Capacitor dielectrics should have a high dielectric constant in order to achieve large values of capacitance per unit area.

In addition, the oxide should have a large free energy of formation so that it will be chemically stable. Tables 1 and 3 show that although tantalum does not have as high a bulk resistivity as titanium, tin oxide, and nichrome, it is possible to prepare stable films having high sheet resistances. In addition, the temperature coefficient of resistance of tantalum is lower than that of many other materials. The value of 25 for the dielectric constant of tantalum oxide, although not as high as that of titania, is adequate for most applications. This combination of good resistor and capacitor properties obtained from tantalum and its oxide led to its selection for the thin film material used to fabricate passive components. It was felt that the

Table 1. [a]Comparison of sheet resistivities and temperature coefficients of metallic thin films

Metal	Sheet resistivity, ohms/square	Temperature coefficient/°C
Au	5.0	0.003
Rh	15.8	0.002
Ni	41.0	0.005
Mo	49.0	0.0002
Ti	59.5	0.0007
Cr	62.0	0.0006
Ta	768.0	<0.0001

[a]From Belser and Hicklin (Ref. 5).

Table 2. Comparison of various oxide materials with respect to dielectric constant and capacitance temperature coefficient

Oxide	Ta_2O_5	Al_2O_3	SiO_2[a]	TiO_2
Dielectric constant, k	25	9	4	100
TCC, ppm/°C	+230	+200	+100	+800

[a]Other oxides usually present and affecting properties.

use of a single metal and its oxide for both the resistors and capacitors would lead to less problems in material compatibility and easier processing than would the selection of different materials, for example tin oxide resistors and evaporated silicon monoxide dielectric capacitors. A comparison was also made between the properties of passive components fabricated from tantalum and tantalum oxide and those fabricated from silicon. This comparison is shown in Table 4, and it can be seen that from the point of view of range of values, tolerance, and temperature coefficient, thin film components compare favorably with those made from silicon.

Table 3. Comparison of resistivity and energy of formation for various metal films and their oxides

Metal	Oxide	Energy of formation $-\Delta G$ K cal/Mole	Resistivity	
			Metal $\times 10^{+16}$	Oxide
Ta	Ta_2O_5	456.4	13.5	10^{16}
Nb	Nb_2O_5	421.8	13.2	10^{6}
Ti	TiO_2	205.9	55.0	10^{10}
Zr	ZrO_2	245.5	44.6	10^{8}
W	WO_3	159.7	5.5	10^{6}
Mo	MoO_3	159.7	5.7	10^{-2}
V	V_2O_5	348.6	26.0	10
Sn	SnO_2	123.8	123.0	10^{-1}
Ni-Cr (80-20)			100.0	

Table 4. Comparison of passive element properties of Ta thin film versus silicon

Resistors				
Material	Max. operating temp., °C	Sheet resistance, ohm/sq.	Temp. coef., ppm/°C	Tolerance, percentage
Ta	200	25 to 1000	0 to −250	0.5 to 10
Si	175	100 to 300	n +250	
			p +600	5 to 20
		1 to 5	+50	
Capacitors[a]				
Dielectric	Stored charge, μ coulomb/cm^2	Time constant, sec	Temp. coef., ppm/°C	Tolerance, percentage
Ta_2O_5	5	2,500	+230	5 to 10
SiO_2	1	3,500	+100	10 to 20
Si (p-n junction)	1–3	0.1		10 to 20

[a]To find capacitance per unit area, divide stored charge by working voltage.

V. FABRICATION OF MICROCIRCUITS USING HYTEK[1] TECHNOLOGY

The major processing steps required are shown in Table 5. The basic semiconductor array, which consists of four transistors and six diodes, is common to all circuits. The circuit function is defined by the last two masking operations which determine the tantalum and final aluminum patterns. This approach leads to considerable economies in production, while placing negligible restrictions on circuit design and configuration.

[1]Coordination of semiconductor and thin film.

Table 5. Fabrication procedure for use with Ta thin films

Manufacturing step	Process control
1. Starting material 18 ± 2 microns 2 ohm cm n-type epitaxially grown silicon on 10–20 ohm cm p-type substrate.	Check layer thickness of material and resistivity of n-type.
2. Oxidize	Check oxide thickness.
3. Apply photo resist, expose to isolation pattern, etch oxide off in isolation areas.	Check pattern dimension after oxide etch.
4. Clean slices and deposit boron "tack-on" impurity.	Measure sheet resistance on unoxidized n-type control slice.
5. Drive in boron to complete isolation.	Check junction depth on control slice.
6. Apply photo resist, expose to transistor base pattern and etch.	Check pattern dimension. Check isolation breakdown.
7. Clean slices and predeposit boron.	Measure sheet resistance on unoxidized n-type control slice.
8. Drive in boron to form collector junction—reoxidize.	Check junction depth and sheet resistance.
9. Apply photo resist, expose to transistor emitter and collector pattern—etch.	Check pattern dimension. Measure collector junction breakdown.
10. Clean slice and predeposit phosphorus.	Check sheet resistance on p diffused unoxidized control slice.
11. Drive in phosphorus to form emitter junction—reoxidize.	Check sheet resistance, junction depth, transistor base width.
12. Apply photo resist, expose to contact pattern and etch oxide.	Check pattern dimensions and registration. Check electrical parameters of transistors and diodes.
13. Clean slides and evaporate aluminum.	Check thickness.
14. Apply photo resist, expose to contact patterns—etch aluminum.	Check pattern dimension and registration.
15. Clean slice and alloy aluminum to silicon.	Check transistor and diode parameters.
AT THIS POINT FABRICATION OF BASIC BLOCK IS COMPLETE.	
16. Evaporate copper.	------
17. Apply photo resist, expose to Ta pattern and etch copper.	Check pattern dimension and registration.
18. Clean slice and evaporate tantalum.	Check tantalum sheet resistance.
19. Each copper to form tantalum pattern.	Check resistor values and capacitor dimensions.
20. Apply photo resist, expose to capacitor and resistor pattern. Anodize tantalum to required voltage and resistance.	Check leakage current and resistance.
21. Evaporate aluminum.	------
22. Apply photo resist to expose counter electrode, conductive paths and contact pads. Etch aluminum.	Check dimensions and capacitor values.
23. Separate into dice, mount on header and bond lead wires to contact pads and header.	Check mechanical strength.
24. First electrical test.	------
25. Hermetic seal	Check for leaks.
26. Second electrical test.	------

The use of readily available n-on-p epitaxial wafers greatly simplifies the problem of electrically isolating the transistors from each other. Steps 1–5 produce islands of n-type material surrounded on all sides and underneath by p-type silicon. Steps 7–11 produce planar type transistors on these islands, protected on the upper surface by various layers of borophosphosilicate glass and by the previous isolation diffusion (steps 1–5), rendering them isolated and independent of their surroundings. Openings are then etched in the glass-like protective coating and aluminum contacts and conducting leads are formed (steps 12–15). The relative inertness of tantalum to acid etches makes the use of a thin film of copper, into which resistor and capacitor patterns have previously been fabricated (steps 16–17), a most suitable method of defining the tantalum thin film components. The thin film of copper defines the unwanted areas and after tantalum evaporation these areas are cleaned using a nitric etch, leaving behind the sharply defined resistor and capacitor patterns of tantalum tenaciously attached to the oxide coatings (steps 18 and 19). Anodization of the tantalum capacitors and resistors is completed in step 20, making use of a previously planned method of interconnection, redundantly connected between individual functional blocks. These interconnections are later severed when scribing and breaking into individual dice. The counter electrodes of the capacitors, together with contact pads and conductive paths, are completed in steps 21 and 22. All that remains is to dice into individual blocks, mount on suitable multipin headers, bond and check (steps 23 and 24). A hermetic seal packaging process and final electrical test complete the procedure (steps 25 and 26).

Figure 9 shows the transistor geometry selected for the implementation of the circuits. Since the circuits nowhere require current handling capabilities in excess of 5 ma, it was decided to fabricate the smallest geometry which could be conveniently employed (Ref. 7). Similar considerations led to the design of the diode geometry shown in Fig. 10. Resistors are fabricated from deposited tantalum which has a final sheet resistance after aging of 200 ohms per square, and most resistors have a 1-mil linewidth. Capacitors are formed by anodizing tantalum to a voltage of 30 v for 2 pF capacitance per mil^2.

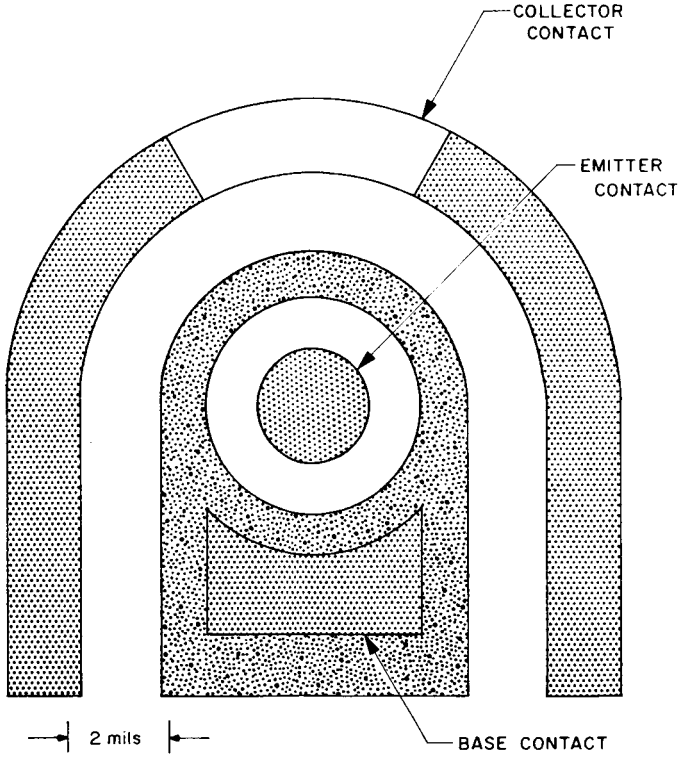


Fig. 9. Transistor structure

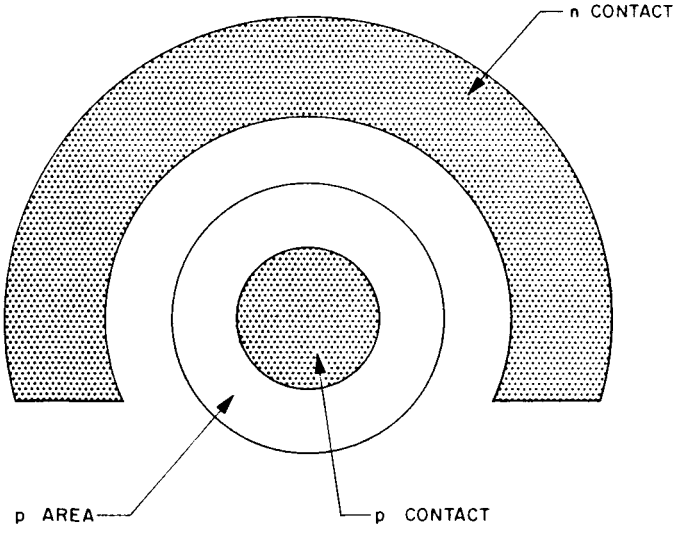


Fig. 10. Diode geometry

VI. RESULTS

The analog-to-digital converter shown in Fig. 1 and 2 has been fabricated in breadboard form, using conventional components and operates as expected. At the present time, fabrication is proceeding in order to produce both flip-flops and gates in microelectronic form. Each process step required for fabrication of the complete integrated circuit has been successfully accomplished and found to be compatible with those process steps immediately preceding and succeeding it. All that remains, therefore, is to carry through the processes from beginning to end. Figure 11 shows a photomicrograph of the basic silicon array. The transistors in this array were tested and found to have current gains in excess of 30 at 1 ma and rise and fall times of 300 and 500 nanoseconds, respectively.

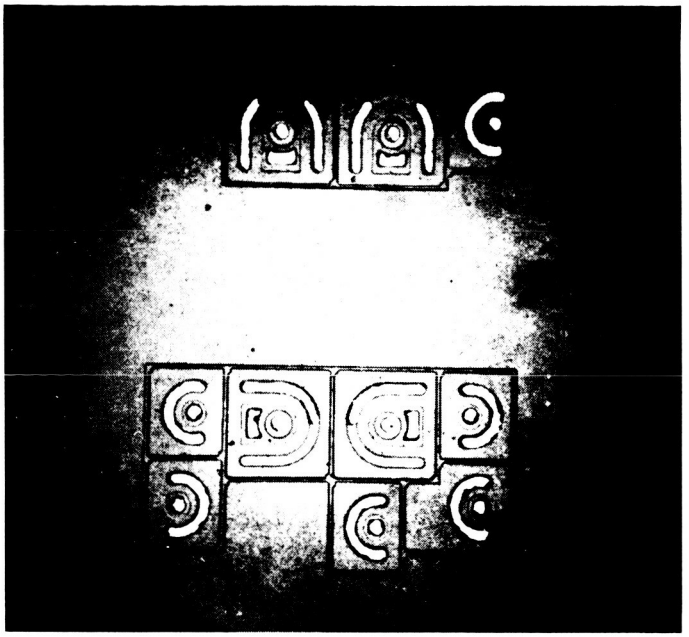


Fig. 11. Photomicrograph of transistors and diodes

Figure 12, a photomicrograph of a partially completed array of flip-flops, shows the basic semiconductor array and superimposed upon it the tantalum pattern required to form the resistors and capacitors. Also shown is the masking provided by areas of photo resist, which will protect portions of the tantalum during the anodization process. Also shown is the pattern of interconnections which connects all the tantalum on one slice so that only one connection to the slice is required in the anodization bath. In order to obtain a complete flip-flop one additional major process step, the evaporation of the aluminum interconnection pattern, is required.

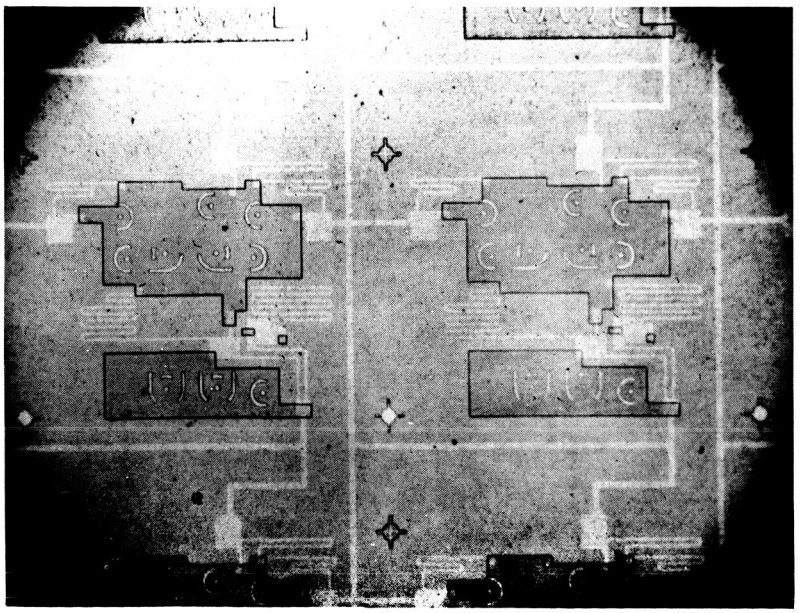


Fig. 12. Photomicrograph showing basic semiconductor pattern with a tantalum pattern deposited on top, followed by the anodization mask

VII. CONCLUSIONS

The design of a 6-bit analog-to-digital converter for fabrication in microelectronic form has been completed. Techniques for the microelectronic fabrication have been discussed, and it has been shown that the combination of semiconductor and thin film techniques offers considerable advantages in the fabrication of this converter and many other microelectronic subsystems.

The contract was terminated for the convenience of the government, due to a lack of funds. Microelectronic gate circuits have been fabricated and tested successfully, but the problem of the aluminum contact on the tantalum oxide capacitor dielectric penetrating through the dielectric and causing a short remains. No JPL funds exist to continue this program, and it is not known whether EOS will continue with their own funds.

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APPENDIX

Evaluation of the Successive Approximation Type of Analog-to-Digital Converter

I. GENERAL DESCRIPTION OF THE PROBLEM

A block diagram of the successive approximation type of ADC is shown in Fig. A-1. In this method of digitizing an analog signal, the digital values appearing in the flip-flop register, which are generated in accordance with the usual successive approximation method, are converted to an equivalent analog signal by switching the precision analog reference voltage into the weighted adder resistor network by means of the precision analog switches. This analog signal, appearing at point a, is fed to the comparator amplifier where it is compared with the analog input signal, appearing at point b. The output of the comparator amplifier is a digital signal indicating that either $a > b$ or $a < b$. If $a = b$, the amplifier will be in a "band of indecision" and its output can be either of the digital levels, and generally will be unpredictable.

In the following analysis it is assumed that there is no error in the input signal.

In order for the ADC to produce a digital value that accurately represents the analog input signal to within $\pm\frac{1}{2}$ of a digital count, the output of the comparator amplifier must switch when the two analog signals are within the voltage equivalent of $\frac{1}{2}$ of a digital count of each other. This then determines the maximum allowable width of the comparator amplifier's band of indecision. In practice, however, the allowable width must be reduced since all of the errors incurred in the analog portion of the ADC must total less than $\pm\frac{1}{2}$ count.

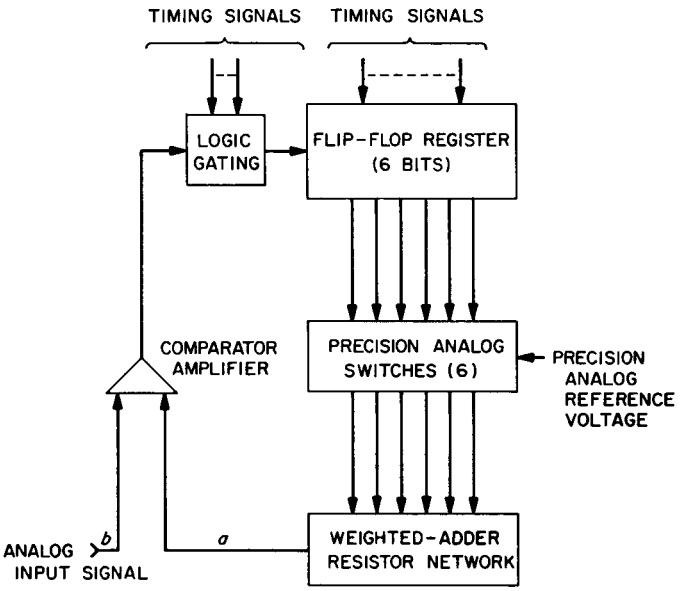


Fig. A-1. Block diagram of the successive approximation type analog-to-digital converter

II. DESCRIPTION OF THE WEIGHTED ADDER RESISTOR NETWORK

The weighted adder resistor network is shown in Fig. A-2. The entire weighted adder network replaced by its Thevenin equivalent is illustrated by Fig. A-3.

e_{out} now becomes

$$e_{out} = \frac{Z_i}{R_{eq} + Z_i}$$

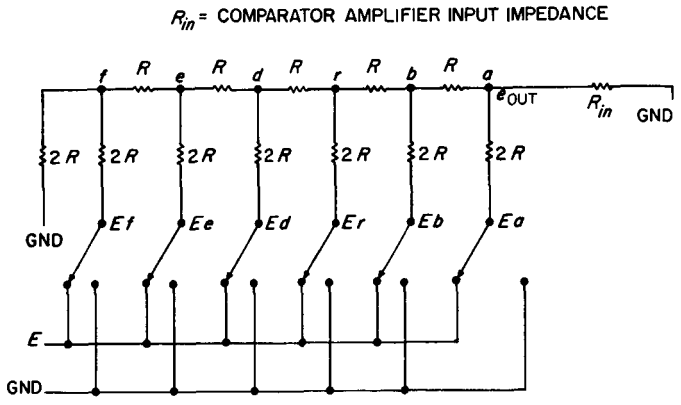


Fig. A-2. The weighted adder resistor network

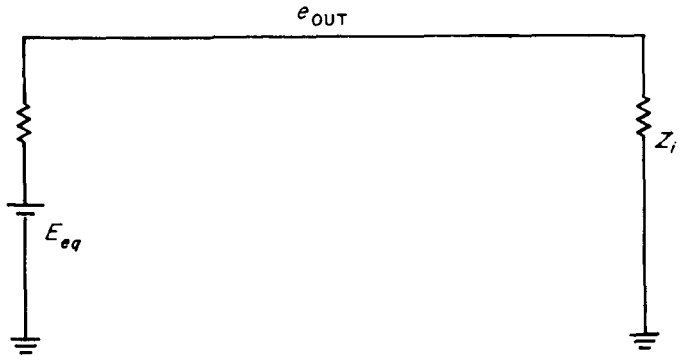


Fig. A-3. Thevenin equivalent of weighted adder resistor network

Thus, it can be seen that the value of Z_i in relation to the value of R_{eq} produces a scaling effect on e_{out}. Otherwise, the value of Z_i does not affect the operation of the weighted adder network, and in order to simplify the calculations involved in analyzing this network, Z_i is assumed to be equal to $2R$.

The Thevenin equivalent of the entire network (including $Z_i = 2R$) at point a, is shown in Fig. A-4 where

$$E_{eq} = \frac{1}{3}\left[\frac{33\ \text{GND}}{32} + E_a + \frac{E_b}{2} + \frac{E_c}{4} + \frac{E_d}{8} + \frac{E_e}{16} + \frac{E_f}{32}\right] \qquad \text{(A-1)}$$

Equation (A-1) shows that the network does sum analog voltage in a manner that will produce an analog signal proportional to a digital binary coded number. The correct relationship between these two quantities will be established if the switches shown in the network in Fig. A-2 are controlled by the flip-flops in the flip-flop register shown in Fig. A-1. The flip-flop holding the most significant bit in the register would be used to control E_a, with E_a being switched to E if the bit is a "1" and E_a being switched to ground if the bit is a "0". The next most significant bit in the register will control E_b in the same manner, and so on for each of the bits in the digital register.

Equation (A-1) contains a ground (GND) term because each end of the network is grounded. These terms were left in the equation to account for the possibility that there could be offsets in these grounds, due to ground loops or some similar phenomena, which would affect e_{out}.

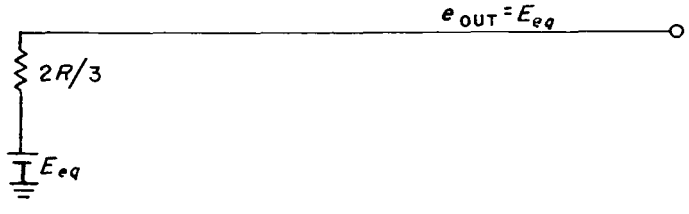


Fig. A-4. Thevenin equivalent of the entire network at point a

The fraction 1/3 appearing in the expression for E_{eq} is the scaling factor produced by the relation between Z_i of the comparator amplifier and the equivalent resistance of the entire weighted adder network, explained above.

Taking Thevenin equivalents for each of the other modes, *b*, *c*, *d*, *e*, and *f* in the same manner as for mode *a*, the following expressions are derived for the voltages at each mode.

$$e_b = \frac{1}{3}\left[\frac{9\ \text{GND}}{16} + \frac{E_a}{2} + E_b + \frac{E_c}{2} + \frac{E_d}{4} + \frac{E_e}{8} + \frac{E_f}{16}\right] \quad \text{(A-2)}$$

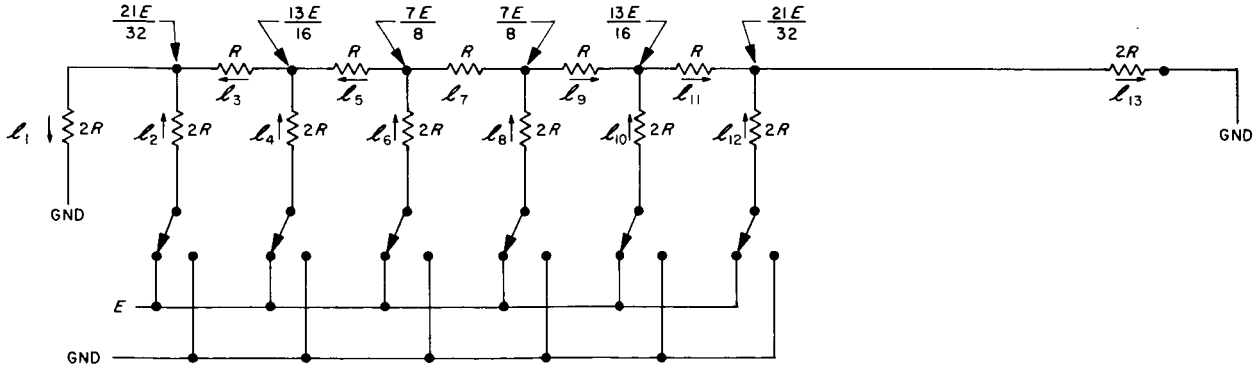
$$e_c = \frac{1}{3}\left[\frac{3\ \text{GND}}{8} + \frac{E_a}{4} + \frac{E_b}{2} + E_c + \frac{E_d}{2} + \frac{E_e}{4} + \frac{E_f}{8}\right] \quad \text{(A-3)}$$

$$e_d = \frac{1}{3}\left[\frac{3\ \text{GND}}{8} + \frac{E_a}{8} + \frac{E_b}{4} + \frac{E_c}{2} + E_d + \frac{E_e}{2} + \frac{E_f}{4}\right] \quad \text{(A-4)}$$

$$e_e = \frac{1}{3}\left[\frac{9\ \text{GND}}{16} + \frac{E_a}{16} + \frac{E_b}{8} + \frac{E_c}{4} + \frac{E_d}{2} + E_e + \frac{E_f}{2}\right] \quad \text{(A-5)}$$

$$e_f = \frac{1}{3}\left[\frac{33\ \text{GND}}{32} + \frac{E_a}{32} + \frac{E_b}{16} + \frac{E_c}{8} + \frac{E_d}{4} + \frac{E_e}{2} + E_f\right] \quad \text{(A-6)}$$

To further demonstrate the functioning of this network, all voltages and currents shown in Fig. A-5 are for a specific example of states of the switches. The example shows all switches set at $+E$, which is the condition when a full-scale digital number is in the flip-flop register. The values shown in Fig. A-5 are based on the assumptions that all resistance values are exact, that the switches are perfect devices, that there is no offset in the ground points, and that the positive voltage $+E$ is exact.



$$\ell_1 = \ell_{13} = \frac{21E}{64R} \qquad \ell_5 = \ell_9 = \frac{E}{16R}$$

$$\ell_2 = \ell_{12} = \frac{11E}{64R} \qquad \ell_6 = \ell_8 = \frac{E}{16R}$$

$$\ell_3 = \ell_{11} = \frac{5E}{32R} \qquad \ell_7 = 0$$

$$\ell_4 = \ell_{10} = \frac{3E}{32R}$$

Fig. A-5. States of the switches

III. ERRORS ENCOUNTERED IN THE SUCCESSIVE APPROXIMATION TYPE OF ANALOG-TO-DIGITAL CONVERTER

Having shown the functioning of the weighted adder resistor network under ideal conditions, the effects caused by nonideal conditions will now be considered.

First, the effects of introducing nonideal switches, offset in the ground points, and a nonexact positive reference voltage are considered. For the moment, the resistance values are still assumed as exact.

Repeating Eq. (A-1) which gave the value of the output voltage from the weighted adder resistor network;

$$e_{out} = \frac{1}{3}\left[\frac{33\ \text{GND}}{32} + E_a + \frac{E_b}{2} + \frac{E_c}{4} + \frac{E_d}{8} + \frac{E_e}{16} + \frac{E_f}{32}\right] \quad \text{(A-7)}$$

This equation is simplified if the idealized condition of no ground offset voltage is applied. It then becomes

$$e_{out} = \frac{1}{3}\left[E_a + \frac{E_b}{2} + \frac{E_c}{4} + \frac{E_d}{8} + \frac{E_e}{16} + \frac{E_f}{32}\right] \text{ (ideally)} \quad \text{(A-8)}$$

Assuming a condition of no ground offset voltage seems to be reasonable, since actual hardware being used indicates that this offset is two to three orders of magnitude less than other errors present in the system.

To further simplify the form of Eq. (A-8) each of the voltage terms E_a, E_b, E_c, E_d, E_e, and E_f can be referred to by a generalized term E_n, where n can be $a, b, c, d, e,$ or f.

Depending on the positions of the switches shown in Fig. A-2, E_n can have either of two values.

$$E_n = O + \Delta_{so} \quad \text{(A-9)}$$

or

$$E_n = E + \Delta_e + \Delta_{se} \quad \text{(A-10)}$$

where

Δ_{so} = offset in a switch in the ground position.

Δ_{se} = offset in a switch in the $+E$ position.

Δ_e = error in the positive reference voltage.

Additional investigation into the hardware used to implement these switches indicates that Δ_{so} will be approximately equal to Δ_{sc}. Therefore, these two possible offsets are considered to be equal and are designated Δ_s.

Examination of Eq. (A-9) and (A-10) shows that more error is introduced when a switch is in the $+E$ position because of the error in the positive reference voltage supply.

Introducing Eq. (A-10) into Eq. (A-8), and making all of the assumptions and approximations previously discussed, then

$$e_{out} = \frac{1}{3}(E + \Delta_e + \Delta_s)$$

$$\left[1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right]$$

$$= \frac{21}{32}(E + \Delta_e + \Delta_s) \qquad \text{(A-11)}$$

Subtracting the idealized value of e_{out}, which is $\frac{21E}{32}$, produces the expression for the total error present in e_{out} due to nonideal switches, ground offsets, and a nonexact positive reference voltage. This expression is

$$e_{out} = \frac{21(\Delta_e + \Delta_s)}{32} \qquad \text{(A-12)}$$

The remaining significant source of error in the weighted adder network must be considered. This source is variations in the values of the resistors used.

Numerous rigorous approaches have been taken to derive an expression for the error produced in e_{out} as the result of variations in the values of the resistances in the weighted adder network. All of these approaches have led to extremely long and cumbersome equations that do not lend themselves to indicating any clear and reasonably simple relationship between the two quantities. As a result, it was decided to investigate the problem experimentally.

Examination of the mathematics describing the weighted adder resistor network shows that when all resistances, including Z_i of the comparator amplifier, change in the same direction by the same percent, the effects of these changes cancel, and no error is produced in the output voltage. Errors are, however, produced when either a single resistor changes value or when all of the R value resistors change by a different amount or in a different direction than the $2R$ resistors (Fig. A-2). Therefore, tests were conducted to simulate these two conditions for various output voltage levels. The results of these tests are summarized in Tables A-1 to A-3.

Other tests, similar to the one whose results are given in Table A-3, were performed with each bit being individually switched in. The worst case, however, is represented by R_{15} in Table A-3 where a resistance change of about 0.9% produced a change in e_{out} of 10 mv out of 3.2810 v ($\approx$ 0.3% v change).

Table A-1. Variations in e_{out} for *R* valued resistances held constant and 2*R* valued resistances varied (+0.1%, +1.0%, −0.1%, −1.0%)

Component	Initial value	Variation in ohms			
R resistors	5,000	+0.1%	+1.0%	−0.1%	−1.0%
2*R* resistors	10,000	10,010	10,100	9,990	9,900
			Variation in e_{out}		
All bits switched in	3.2818	3.2821	3.2842	3.2816	3.2789
2^5 bit only switched in	1.6664	1.6661	1.6630	1.6672	1.6705
2^4 bit only switched in	0.8333	0.8334	0.8343	0.8334	0.8325
2^3 bit only switched in	0.4166	0.4168	0.4185	0.4165	0.4148
2^2 bit only switched in	0.2082	0.2084	0.2099	0.2081	0.2066
2^1 bit only switched in	0.1040	0.1042	0.1052	0.1040	0.1029
2^0 bit only switched in	0.0520	0.0521	0.0527	0.0519	0.0512

Table A-2. Variations in e_{out} for 2*R* valued resistances held constant and *R* valued resistances varied (+0.1%, +1.0%, −0.1%, −1.0%)

Component	Initial value	Variation in ohms			
R resistors	5,000	5,005	5,050	4,995	4,950
2*R* resistors	10,000	+0.1%	+1.0%	−0.1%	−1.0%
			Variation in e_{out}		
All bits switched in	3.2818	3.2821	3.2799	3.2823	3.2844
2^5 bit only switched in	1.6664	1.6672	1.6709	1.6665	1.6629
2^4 bit only switched in	0.8333	0.8334	0.8328	0.8337	0.8343
2^3 bit only switched in	0.4166	0.4166	0.4150	0.4170	0.4186
2^2 bit only switched in	0.2082	0.2082	0.2068	0.2085	0.2100
2^1 bit only switched in	0.1040	0.1040	0.1030	0.1043	0.1053
2^0 bit only switched in	0.0520	0.0520	0.0512	0.0521	0.0529

Table A-3. Changes required in resistances to produce increases and decreases of 10 mv in e_{out} for all bits in, and for $E = +5$ vdc

Resistor	To make e_{out} increase by 10 mv from 3.2810 to 3.2910 v		To make e_{out} decrease by 10 mv from 3.2810 to 3.2710 v	
	Value, ohms	% Change	Value, ohms	% Change
R_{15}	10,094	+ 0.94	9,907	− 0.93
R_{13}	9,832	− 1.68	10,182	+ 1.82
R_{11}	9,400	− 6.00	10,680	+ 6.80
R_{10}	5,200	+ 4.00	4,800	− 4.00
R_9	8,320	−16.80	12,270	+ 22.70
R_8	6,000	+20.00	4,100	− 18.00
R_7	7,000	−30.00	15,100	+ 51.00
R_6[a]				
R_5	6,300	−37.00	17,710	+ 77.10
R_4	2,000	−60.00	10,030	+100.60
R_3	6,100	−39.00	18,900	+ 89.00
R_2	2,400	−52.00	8,900	+ 78.00
R_1	13,800	+38.00	7,510	− 24.90

[a]Due to the symmetrical nature of the network there is ideally no current flow through R_6 with all bits switched in. Because of this, varying R_6 produced no measurable effect in e_{out}.

IV. SUMMARY OF EVALUATION

To summarize the analysis, values currently anticipated for use in the system being constructed are inserted into the expressions derived.

In the system under construction E is to be +5.000 v. The value of one count at the output of the weighted adder resistor network is

$$\frac{5.000}{64} \times \frac{21}{32} = \frac{105.000}{2048} \approx 51.27 \text{ mv.}$$

The 1/2 count allowable error presented to the comparator amplifier is then 25.63 mv.

From Eq. (A-13) the error introduced into e_{out} due to nonideal switches, ground offsets, and a nonexact positive reference voltage is

$$\Delta_{e_{out}} = \frac{21\,(\Delta_E + \Delta_s)}{32} \qquad \text{(A-13)}$$

Taking $+E$ to be nominally 5 v provided by a 0.1% power supply, $\Delta_E = 5$ mv.

Experimental data indicate that switch offset Δ_s is in the order of 8 mv. Therefore,

$$\Delta_{e_{out}} = \frac{21\,(5 + 8)}{32} \text{ mv} = 8.53 \text{ mv.}$$

From the experimental results given in Table A-3, constructing the weighted adder resistor network with 1% resistors should introduce an additional error in the order of 11 mv. Therefore, the total foreseeable error at the output of the weighted adder resistor network is in the order of 19.5 to 30 mv, which is well under the allowable error of 25.63 mv.